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EXAMINER	
GOODWIN, DAVID J	

ART UNIT	PAPER NUMBER
2818	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/542,720	VISSER ET AL.	
	Examiner	Art Unit	
	David Goodwin	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 14 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

3. The specification does not disclose that the capacitance is independent of the gate.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 4 is rejected to because of the following informalities: The claim specifies that the ratio is substantially equal to one. However, one lies outside of the claimed range of $1<c/c<2$. Appropriate correction is required.

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Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 through 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (US 6,291,298).

3. Regarding claim 1

4. Williams teaches an insulated gate device comprising a gate connected to a gate terminal (fig 6c) and having a variable input capacitance means adjacent at the gate terminal (fig 7H) as the device is switched between an off and an on state, a ratio between a final value of the capacitance when the device is on and the initial value of the capacitance when the device is off is smaller than 2.0 (column 4 lines 60-67).

5. The power MOSFET has a very low input capacitance both in its on and in its off state. This is proved by fig 7E which shows the slope of Q-Vgs which is inversely proportional, in the first approximation to the input capacitance. In particular, from the cited figure the slope of the curve can be extrapolated before the so called Miller Plateau, when the device is still in its off state and after the Miller Plateau when the Vgs is above the threshold voltage and an inversion layer has formed in the channel region, i.e. when the device is in its on state. From these data a ratio Ciss-on/Ciss can be extrapolated. The dashed line indicates ideal behavior, substantially equal to 1, it is

preferred that the device adhere to ideal behavior as closely as possibly in order to minimize power loss (fig 7E) (column 5 lines 1-10).

6. Regarding claim 1 fails to specify the optimized capacitance ratio. However, differences in capacitance ratio will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such ratio are critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955). MPEP 2144.05.II.

7. Further, the limitation must distinguish from the prior art in terms of structure rather than function, *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also *In re Swinehart*, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971). Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Danly*, 263 F. 2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F. 2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

8. Regarding claim 2.

9. Williams teaches the device comprises a power MOSFET (fig 7a) (column 8 lines 15-25).

10. Regarding claim 3.

11. Williams teaches the behavior as shown by the dashed line (fig 7E) has a ratio of less than 1.5.

12. Regarding claim 4.

13. Williams teaches the behavior as shown by the dashed line (fig 7E) if ideal has a ratio of substantially equal to 1 (column 4 lines 55-65).

14. Regarding claim 5.

15. Williams teaches the device comprises a capacitor connected between the gate terminal and the gate of the device (fig 7H).

16. Regarding claim 6.

17. The MOSFET has a vertical structure in that the gate and the source of the device are on one face of the chip body of the device and the drain of the MOSFET is provided on the opposite face of the chip body (fig 6c-6e). The variable input capacitance means comprises a capacitor between the gate terminal and the gate of the device (fig 7g,h)

18. Regarding claim 7.

19. Williams teaches the capacitor is integrated on the chip body (fig 7G, 7H).

20. Regarding claim 8.

21. Williams teaches The device comprises a capacitor, said capacitor is superimposed on the gate of the MOSFET (fig 7G, 7H).

22. Regarding claim 10.

23. Williams teaches that the gate is connected to a fourth terminal of the device (fig 6C).

24. The applicant does not specify the location or relation of the fourth terminal as opposed to any other terminal. Therefore the broadest reasonable interpretation of a

fourth terminal is that it may comprise the source or drain terminals as illustrated in figure 6c).

25. Regarding claim 12.

26. Capacitors comprise an insulating layer at the gate (fig 7G, 7H).

27. Regarding claim13.

28. Williams teaches the capacitor is in integrated with the gate (fig 7G, 7H).

29. Regarding claim 15.

30. Williams teaches an insulated gate device comprising a gate, the device having a capacitance at the gate (fig 6c), the value of the capacitance is a function of an effective thickness of an insulating layer at the gate (fig 7H), the effective thickness of the insulation layer being selected to ensure that a ratio between a final value of the capacitance when the device is on and the initial value of the capacitance when the device is off is smaller than or equal to a second ratio of a maximum charge receivable on the gate and a charge required to reach a threshold voltage of the gate (see fig 7E, wherein the ratio are embodied by the slope of the lines) (column 4 lines 60-67).

31. The power MOSFET has a very low input capacitance both in its on and in its off state. This is proved by fig 7E which shows the slope of Q-Vgs which is inversely proportional, in the first approximation to the input capacitance. In particular, from the cited figure the slope of the curve can be extrapolated before the so called Miller Plateau, when the device is still in its off state and after the Miller Plateau when the Vgs is above the threshold voltage and an inversion layer has formed in the channel region, i.e. when the device is in its on state. From these data a ratio Ciss-on/Ciss can be

extrapolated. The dashed line indicates ideal behavior, substantially equal to 1, it is preferred that the device adhere to ideal behavior as closely as possibly in order to minimize power loss (column 5 lines 1-10).

32. The limitation must distinguish from the prior art in terms of structure rather than method of making, *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also *In re Swinehart*, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971).

33. Further, the limitation must distinguish from the prior art in terms of structure rather than function, *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also *In re Swinehart*, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971). Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Danly*, 263 F. 2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." *Hewlett-Packard Co. v. Bausch & Lomb Inc.,* 909 F. 2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

34. Regarding claim 16

35. Williams teaches an insulated gate device having a capacitance.

36. The insulated gate device comprising a gate. The device capacitance at the gate (fig 7H) where the value of the capacitance is a function of an effective thickness of an insulation layer at the gate, the effective thickness of the insulation layer being selected to ensure that a first ratio between a final value of the capacitance when the device is on and the initial value when the device is off is smaller or equal to a second ratio of a

maximum voltage applicable to the gate and the threshold voltage required on the gate to switch the device (the ratios are embodied by the slopes of the lines of the first part and second part of the figure which if idealized would be one, see fig 7E) (column 4 lines 60-67).

37. The power MOSFET has a very low input capacitance both in its on and in its off state. This is proved by fig 7E which shows the slope of Q-Vgs which is inversely proportional, in the first approximation to the input capacitance. In particular, from the cited figure the slope of the curve can be extrapolated before the so called Miller Plateau, when the device is still in its off state and after the Miller Plateau when the Vgs is above the threshold voltage and an inversion layer has formed in the channel region, i.e. when the device is in its on state. From these data a ratio Ciss-on/Ciss can be extrapolated. The dashed line indicates ideal behavior, substantially equal to 1, it is preferred that the device adhere to ideal behavior as closely as possibly in order to minimize power loss (column 5 lines 1-10).

38. The limitation must distinguish from the prior art in terms of structure rather than method of making, *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also *In re Swinehart*, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971).

39. Further, the limitation must distinguish from the prior art in terms of structure rather than function, *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also *In re Swinehart*, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971). Claims directed to apparatus must be distinguished from the

prior art in terms of structure rather than function. *In re Danly*, 263 F. 2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F. 2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

40. Regarding claim 17

41. Williams teaches an insulated gate device having a capacitance.

42. An insulated gate device comprising a gate and an insulation layer at the gate, the layer having an effective thickness of at least a quotient of a device parameter and a ratio of maximum charge accomodatable on the gate and a minimum charge required on the gate for complete switching minus one(fig 6c), the device parameter being equal to the product of an effective gate capacitance area and a difference between an inverse of a first value of a gate capacitance of the insulated gate device, that is when the device is off and an inverse of a second value of the gate capacitance that is when the device is on (fig 7H) (the formulae of the capacitance ratios are embodied in the slopes of the graph of fig 7E) (column 4 lines 60-67).

43. The power MOSFET has a very low input capacitance both in its on and in its off state. This is proved by fig 7E which shows the slope of Q-Vgs which is inversely proportional, in the first approximation to the input capacitance. In particular, from the cited figure the slope of the curve can be extrapolated before the so called Miller Plateau, when the device is still in its off state and after the Miller Plateau when the Vgs is above the threshold voltage and an inversion layer has formed in the channel region, i.e. when the device is in its on state. From these data a ratio Ciss-on/Ciss can be

extrapolated. The dashed line indicates ideal behavior, substantially equal to 1, it is preferred that the device adhere to ideal behavior as closely as possibly in order to minimize power loss (column 5 lines 1-10).

44. The limitation must distinguish from the prior art in terms of structure rather than method of making, *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also *In re Swinehart*, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971).

45. Further, the limitation must distinguish from the prior art in terms of structure rather than function, *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also *In re Swinehart*, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971). Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Danly*, 263 F. 2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F. 2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

46. Regarding claim 18

47. Williams teaches an insulated gate device having a capacitance.

48. Williams teaches an insulated gate device comprising a gate connected to a gate terminal (fig 6c) and having a variable input capacitance means adjacent at the gate terminal (fig 7H) as the device is switched between an off and an on state, a ratio between a final value of the capacitance when the device is on and the initial value of the capacitance when the device is off is smaller then 2.0 (column 4 lines 60-67).

49. The power MOSFET has a very low input capacitance both in its on and in its off state. This is proved by fig 7E which shows the slope of Q-Vgs which is inversely proportional, in the first approximation to the input capacitance. In particular, from the cited figure the slope of the curve can be extrapolated before the so called Miller Plateau, when the device is still in its off state and after the Miller Plateau when the Vgs is above the threshold voltage and an inversion layer has formed in the channel region, i.e. when the device is in its on state. From these data a ratio Ciss-on/Ciss can be extrapolated. The dashed line indicates ideal behavior, substantially equal to 1, it is preferred that the device adhere to ideal behavior as closely as possibly in order to minimize power loss (column 5 lines 1-10).

50. Further, the limitation must distinguish from the prior art in terms of structure rather than function, *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also *In re Swinehart*, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971). Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Danly*, 263 F. 2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." *Hewlett-Packard Co. v. Bausch & Lomb Inc.,* 909 F. 2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

51. Regarding claim 19.

52. The limitation must distinguish from the prior art in terms of structure rather than function, *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also *In re Swinehart*, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA

1971). Claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Danly*, 263 F. 2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F. 2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

53.

54. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (US 6,291,298) as applied to claim 5 above and further in view of Jones (US 4,683,387).

55. Regarding claim 9 and ~~14~~ 11,

56. Williams teaches elements of the claimed invention above. Williams does not teach that the capacitor is a discrete element.

57. Jones teaches that a discrete gate to source capacitor may be included (column 2 lines 25-35).

58. It would have been obvious to one of ordinary skill in the art to incorporate a discrete capacitor between the gate and a gate terminal in order to reduce the Miller effect thereby reducing the power loss and improving the device frequency.

59. Regarding claim 11.

60. Williams teaches the device package further comprises a bias (fig 6D). Said bias is supplied along conductive paths (fig 6D) and all conductive paths provide a resistance.

Response to Arguments

61. Applicant's arguments with respect to claims 1 through 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

62. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Goodwin whose telephone number is (571)272-8451. The examiner can normally be reached on Monday through Friday, 9:00am through 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571)272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJG

STEVEN LOKE
SUPERVISORY PATENT EXAMINER